REMARKS

Applicant thanks the examiner for her time and help during the examiner interview conducted by phone on May 17, 2006, in which the examiner agreed to remove the finality of the March 28, 2006, Office Action. Applicant filed with the United States Patent Office a Statement of Substance of Interview, dated May 22, 2006, in which applicant summarized what applicant understood was agreed upon in relation to the finality status of the March 28, 2006, Office Action.

Applicant amended independent claim 1 to include the feature that the coupling out of radiation occurs through the void, and that the void extends only partially through the radiation transmissive window. Support for the added features is provided throughout the originally filed application, including, for example, in FIGS. 1A and 2, at page 14, lines 21-26, page 18, line 25, to page 19, line 6, page 20, lines 21-24, etc.

In addition, applicant canceled independent claim 27 and added new independent claim 28 which recites features similar to those recited in old independent claim 1 and in claims 5 and 6.

The examiner rejected claim 1-27 under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in combination with U.S. Patent No. 6,541,799 to Udagawa (erroneously identified in the office action as U.S. Patent No. 6,541,790), or Japanese reference No. 61-110476 (assigned to NEC Corp), or U.S. Patent No. 6,239,033 to Kawai.

Applicant notes that the examiner did not explicitly identify what is being considered as the alleged admitted prior art. At one point the examiner makes reference to paragraphs 2-14 of applicant's specification, and at another point reference is made to Krames (by which applicant assumes the examiner is referring to U.S. Patent No. 6,229,160 to Krames.) Applicant therefore asks that should the examiner decide to continue relying on anything discloses in applicant's own specification as a basis for subsequent rejections, that the particular basis upon which such rejections are made be more clearly identified to enable applicant to better know the case it has to meet, and thereby address the specific bases of rejection.

Applicant further notes that the examiner did not initial PTO-1449 form on which applicant cited Japanese reference No. 61-110476 (the reference upon which the examiner is now relying upon). Applicant asks that the examiner initial the PTO-1449 on which this reference was cited, and forward a copy thereof the applicant's representative for service.

With reference to the various rejections raised in the office action, applicant submits that none of the cited prior art references discloses or suggests "said second main surface having at least one void selected from the group consisting of a trench recess and a pit recess formed therein for increasing a coupling-out of radiation from said window through said void wherein said void extends only partially through said window," as required by independent claim 1. Applicant further submits that in relation to the examiner's rejection of the claims as being obvious over the alleged admitted prior art in view of Udagawa, no motivation to combined the alleged admitted prior art and Udagawa exists.

Obviousness Rejections Over the Alleged Admitted Prior Art and Udagawa

With respect to the examiner's rejections of the claims as being obvious over the alleged admitted prior art and Udagawa, the examiner referred to paragraphs 2-14 of applicant's specification. These paragraphs describe the use of a SiC substrate (see paragraph 3-4 of US 2004/0046179). SiC is a substrate material which is particularly suitable for GaN-based semiconductor materials because of the small lattice mismatch with respect to GaN-based material. As described in, for example, an excerpt from the book "Physics of Semiconductor Devices" by S. M. Sze (a copy of the excerpt is attached herein for the examiner's reference), SiC generally has a lattice constant of 3.1Å, while GaN generally has a lattice constant of approximately 3.2Å. The respective lattice are thus mismatched by 0.1Å. Furthermore, SiC and GaN have similar crystal structure, which facilitates GaN growth on SiC.

As will be explained in greater details below, Udagawa describes a group-III nitride semiconductor LED having a Si single crystal as a substrate (col. 1, lines 13-15). Unlike SiC material, Si generally has a lattice constant of approximately 5.4Å, which is far greater than the lattice constant of SiC. Also, the crystal structure of Si differs from the crystal structure of GaN. The lattice mismatch between Si and GaN as well as the differing crystal structures between the two materials complicates the growth of GaN material on the Si material.

Accordingly, due to the unsuitability of using Si with GaN, there would be no motivation for a person skilled in the art to combine the alleged admitted prior art with Udagawa. Indeed, unlike Udagawa's teaching of removing as much as the substrate as possible so as to eliminate material stress, a SiC substrate does not have to be entirely removed because the better matched lattice constants of SiC and GaN do not result in the type of material stress experience by Udagawa's devices. Thus, Udagawa's objective of removing substrate materials because of material mismatch while still maintaining mechanical stability in the device is inapplicable to the alleged admitted prior art.

Because there is no motivation to combine the alleged prior art with Udagawa, the examiner's has thus failed to establish a prima facie case of obviousness with respect to independent claim 1. Applicant's independent claim 1 is therefore patentable over the alleged admitted prior art and Udagawa.

Additionally, neither paragraphs 2-14 of applicant's specification, nor U.S. Patent No. 6,229,160 to Krames mentioned in these paragraphs (which applicant does not admit is prior art, and reserves the right to show an earlier invention date than Krames' priority date), discloses or suggests at least "said second main surface having at least one void selected from the group consisting of a trench recess and a pit recess formed therein for increasing a coupling-out of radiation from said window through said void wherein said void extends only partially through said window."

Particularly, paragraphs 2-14 of applicant's specification describe a rectangular substrate 19 that has no void or any types of indentations or depressions. Thus, paragraphs 2-14 of applicant's specification do not disclose or suggest at least "said second main surface having at least one void selected from the group consisting of a trench recess and a pit recess formed therein for increasing a coupling-out of radiation from said window through said void wherein said void extends only partially through said window," as required by applicant's independent claim 1.

Krames describes a light emitting device (LED) having an active region of epitaxial layers 10 (col. 3, line 66 to col. 5, line 2 and FIG. 2). As explained in applicant's Amendment in Reply to Action of March 25, 2005, Krames' LED includes a top window layer 12 and a bottom window layer 13 (col. 4, lines 17-28 and FIG. 2). Top window layer 12 has a surface attached to

epitaxial layers 10 and a top surface 17 opposite the surface attached to epitaxial layers 10. Top surface 17 has no void. Bottom window layer 13 has a surface attached to epitaxial layers 10 and a surface to which an electrical contact 15 is attached (col. 4, lines 33-36). The surface with electrical contact 15 is opposite the surface attached to epitaxial layers 10 and has no void.

As also explained in applicant's Amendment in Reply to Action of March 25, 2005, although FIG. 7 shows a cavity between two adjacent devices formed on a wafer, that is not the void in the transmissive window recited in applicant's claim 1. Rather, this cavity corresponds to the area that includes the material that is wasted during a dicing operation of the wafer to form multiple devices (col. 6, line 47 to col. 7, line 24).

Accordingly, Krames does not describe a window including a second main surface having a void, and therefore Krames does not disclose or suggest at least "increasing a coupling-out of radiation from said window through said void," and/or "said void extends only partially through said window," as required by applicant's independent claim 1.

As noted above, Udagawa describes a group-III nitride semiconductor LED having a Si single crystal as a substrate (col. 1, lines 13-15). To increase the light emission intensity, Udagawa describes eliminating the Si substrate except for the part on which a back surface electrode is disposed. Specifically, Udagawa explains that "[t]he Si single crystal in the region where an ohmic electrode (a back surface electrode=first electrode) is laid on the back surface of the Si single crystal substrate is allowed to remain, and the Si single crystal material in the other regions is removed using a known etching technique. When the substrate material in the region where the back surface electrode (first electrode) is present is allowed to remain, an effect of more firmly supporting the LED is attained using the mechanical strength of the remaining substrate material, as compared with the case of removing the entire substrate" (col. 4, lines 50-59). Udagawa further indicates that its motivation for removing substrate material is to reduce the mismatch between the Si substrate and the group-III nitride semiconductor material disposed on the substrate.

Thus, Udagawa seeks to remove as much as the Si substrate as it can without compromising the structural integrity of the LED device. Accordingly, as shown in Udagawa's FIG. 5, the substrate 101 is etched to form perforated part 109. Electrode 110 is disposed on the non-etched part of the substrate 101 (col. 12, lines 6-26). Udagawa then explains "[t]he

perforated part 109 was formed by etching and thereby eliminating the Si single crystal using a mixed solution of hydrofluoric acid (HF) and nitric acid (HNO3). The depth of the perforated part 109 was set to about 300 μm corresponding to the layer thickness of the substrate 101" (col. 12, lines 10-15.)

In other words, the perforated part 109 of Udagawa's LED extends along the entire thickness of the substrate so as to remove as much of the substrate material as possible. Udagawa, therefore does not describe or suggests at least "wherein said void extends only partially through said window."

Additionally, at no point does Udagawa describe that any light emission passes through the perforated part 109. Thus, Udagawa also does not disclose or suggest at least the feature of "increasing a coupling-out of radiation from said window through said void," as required by applicant's independent claim 1.

Thus, because none of paragraphs 2-14 of applicant's specification, Krames, and Udagawa discloses or suggests, alone or in combination, at least the features of "increasing a coupling-out of radiation from said window through said void," and/or "wherein said void extends only partially through said window," applicant's independent claim 1 is patentable over these prior art references.

Obviousness Rejections Over the Alleged Admitted Prior Art and JP61-110476

As noted, the examiner also rejected independent claim 1 as being obvious over the alleged admitted prior art in view of Japanese reference No. 61-110476.

As explained above, neither paragraphs 2-14 of applicant's specification, nor Krames discloses or suggests at least "increasing a coupling-out of radiation from said window through said void," and/or "said void extends only partially through said window."

Japanese reference No. 61-110476 describes an infrared LED in which a GaAs substrate is perforated, except where an electrode contacts the substrate, to form recesses. Specifically, the reference describes:

> **Further, the portion that GaAs crystal 1 except the electrode 5 of the back surface is exposed is perforated with at etchant, or treated to form irregular state, thereby increasing the reflection in a random direction except the vertical in the reflection on the surface A to increase the producing efficiency from the side. Thus, low contacting resistance and high emitting light output can be obtained as a whole (Abstract)**

Thus, the recesses described in the above reference are configured to reflect and not transmit radiation. The recesses direct the reflected radiation either to the surface opposite the recesses or to the side surfaces of the device. The recesses, therefore, do not cause radiation generated by the device to be coupled out through them. Accordingly, Japanese reference No. 61-110476 does not disclose or suggest at least "said second main surface having at least one void selected from the group consisting of a trench recess and a pit recess formed therein for increasing a coupling-out of radiation from said window through said void," as required by applicant independent claim 1. Accordingly, applicant's independent claim 1 is patentable over the alleged admitted prior art and Japanese reference No. 61-110476.

While reviewing the 61-110476 reference, applicant noticed that the abstract page of Japanese patent reference No. 03227078 was appended to the electronic copy of the 61-110476 patent available on the USPTO's PAIR system. Because applicant was not certain whether the examiner relied on this reference or the 61-110476 reference in forming the examiner's basis for rejecting applicant's claims, applicant considered this reference as well, and believes that the combination of the alleged admitted prior art and the 03227078 reference also does not establish a prima facie case of obviousness for rejecting independent claim 1. Applicant also submits herewith a supplemental IDS in which the 03227078 reference is cited.

Japanese Reference No. 03227078 describes an N-type semiconductor layer 2 and a P-type semiconductor grown on an N-type GaAs substrate 1. A V-shaped groove is etched in GaAs substrate (see Abstract page). At no point, however, does this reference indicate that generated light is coupled out through the groove. Thus, Japanese Reference No. 03227078 fails to disclose at least the feature of "said second main surface having at least one void selected from the group consisting of a trench recess and a pit recess formed therein for increasing a coupling-out of radiation from said window through said void," as required by applicant independent claim 1.

As explained above, paragraphs 2-14 of applicant's specification and Krames also fail to disclose or suggest at least "said second main surface having at least one void selected from the group consisting of a trench recess and a pit recess formed therein for increasing a coupling-out of radiation from said window through said void," as required by applicant independent claim 1.

Accordingly, applicant's independent claim 1 is also patentable over the alleged admitted prior art and Japanese Reference No. 03227078.

Obviousness Rejections Over the Alleged Admitted Prior Art and Kawai

Finally, the examiner also rejected independent claim 1 as being obvious over the alleged admitted prior art in view of Kawai.

As explained in applicant's July 25, 2005, Reply to Action of March 25, 2005, Kawai describes a method for manufacturing a semiconductor device in which the bottom surface of a sapphire or silicon substrate is etched so as to improve the high frequency operation and/or high-power output of the device (col. 3, lines 26-35).

Kawai describes devices are understood to be edge-emitting lasers (FIGS. 1 and 14). Kawai provides no motivation to modify the window of Krames with a recess at least because Kawai's devices emit radiation through a cavity edge rather than a window. For example, the device of Kawai FIG. 14 is understood to emit light through an edge of an active layer 55 not through a window layer.

Moreover, no device of Kawai has window with a recess as presently claimed. For example, the Kawai FIG. 14 device has a via hole 61 in a sapphire substrate to permit ohmic contact between an electrode layer 62 and a GaN layer 53. Sapphire substrate 61 is not the presently claimed window at least because substrate 61 has no second main surface opposite a first main surface with the second main surface having a recess.

Thus, because Kawai does not discloses or suggests a window of the component as set forth in claim 1, Kawai also does not disclose or suggest at least "increasing a coupling-out of radiation from said window through said void," or "said void extends only partially through said window," as required by applicant's independent claim 1. As explained above, the alleged admitted prior art also does not disclose at least these features. Accordingly, applicant's independent claim 1 is patentable over the admitted prior art and Kawai.

For the foregoing reasons, applicant's independent claim 1 is patentable over the various prior art references cited by the examiner.

Claims 2-26 depend from independent claim 1, and are therefore patentable for at least the same reasons as independent claim 1.

Obviousness Rejection of Claims 5 and 6

In addition, the examiner also rejected claim 6 as under 35 U.S.C §103(a) over the alleged admitted prior art, and in view of Udagawa, JP61-110476, or Kawai.

Claim 6 recites "[t]he semiconductor component according to claim 5, wherein said angle is between 20° and 70°." Claim 5 recites "[t]he semiconductor component according to claim 1, wherein said void has at least one planar side surface enclosing an angle different from 90° with said second main surface.

The examiner admitted that "[a]dmitted prior art does not disclose transmissive window ..., wherein window have side surface and having an angle range of 20-70 degrees" (emphasis in the Office Action, page 3). The examiner, however, failed to explain in what prior art references the feature pertaining to the angle of 20-70 degrees is disclosed.

Although the various prior art references relied upon by the examiner (including Udagawa, JP61-110476, and/or Kawai) describe perforations and/or recesses used for various purposes (e.g., in Udagawa the perforation was formed to minimize the volume of the substrate material that is used with the substrate to thereby reduce the stress in the semiconductor layers applied on the substrate), none of those prior art references mentions an angle enclosed by a planar side surface and another surface of the perforations or recesses that is between 20-70 degrees. Accordingly, none of the references cited by the examiner discloses or suggests at least the feature of the void having at least one planar side surface enclosing an angle with said second main surface, "wherein said angle is between 20° and 70°," as required by applicant's claim 6. Accordingly, applicant's claim 6 is therefore patentable over the cited prior art.

Applicant's independent claim 28 recites "wherein said void has at least one planar side surface enclosing an angle between 20° and 70° with said second main surface." For reasons similar to those provided with respect to claim 6, independent claim 28 is patentable over the cited prior art.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing remarks, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicants have (a) addressed certain comments of the examiner does not mean that the applicants concede other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicants concede any of the examiner's positions with respect to that claim or other claims.

No fee is believed due. Please apply any other charges to deposit account 06-1050, referencing 12406-118US1.

Respectfully submitted,

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